Error Detection Circuits

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Error Detection Circuits Michael Gössel,Steffen Graf,1993 The first comprehensive description of systematic methods for designing optional error detection circuits Table of Contents Overview and Introduction Combinatorial Error Detection Circuitry Sequential Error Detection Circuits Design Algorithms for Error Detection Circuits Appendix References Index 100 illustrations **Error Detecting Logic for Digital Computers** Frederick F. Sellers,Muyue Xiao,Mu-yüeh Hsiao,Leroy W. Bearnson,1968 Error Detection, Decoding, and Error Correction for Circuit Codes John Christopher Beebee,1972

Concurrent Error Detection Steven Scott Gorshe,2002 Concurrent error detection CED is the detection of errors or faults in a circuit or data path concurrent with normal operation of that circuit The general approach for CED is to calculate a check symbol for the inputs to the circuit under operation predict the check symbol that will result for the output of the circuit for those inputs and compare the predicted check symbol to the one that is actually calculated for the output If the predicted and actual check symbols are different an error or fault has been detected The alternative to this check symbol prediction is to use a second copy of the circuit under operation and compare the results of the two circuits For some classes of circuits the prediction of the output check symbol can require less circuitry than a second copy of the circuit being tested Four examples of these types of circuits are examined in this dissertation Arithmetic Logic Units ALUs array multipliers self synchronous scrambler descrambler pairs with their intervening data path and switch fabrics Faults in integrated circuits tend to produce unidirectional errors Unidirectional errors are those in which all of the errors are in the same direction e g 0 to 1 errors within the block of data covered by a given check symbol For this reason codes that are optimized for unidirectional errors are the focus of investigation for most of the applications In particular the Bose Lin codes are examined for those applications where unidirectional errors are expected to be typical In order to examine the performance of the Bose Lin codes in one of these applications it was necessary to determine the theoretical performance for Bose Lin codes for error rates beyond what had been previously studied This analysis of Bose Lin codes with large numbers of burst errors also included a further generalization of the codes مدخل لدراسة اسئلة **CRL** القيمة المطلقة محمد اسماعيل عبد العظيم الاشهب 2010, الاكاديمية الحديثة للكتاب الجامعي هذا **A Concurrent Timing Error Detection Circuit for CMOS** Christopher G. Knight,1997 An Ultra-Fast All-Optical Error Detection and Correction Circuit Based on Spectral Logic ,2000 All optical logic circuits based on the polarization properties of non degenerate four wave mixing are proposed It is shown that higher level Boolean operations involving several bits can be implemented without resorting to the standard 2 input gates As a simple illustration of the idea a circuit performing error correction on a 3 1 Hamming Code is demonstrated Error free performance Bit Error Rate of Logic Synthesis for Concurrent Error Detection Stanford University. Computer Systems Laboratory,Nur A. Touba,Edward J. McCluskey,1993 Abstract The structure of a circuit determines how the effects of a fault can propagate and hence affects the cost of concurrent error detection By considering circuit structure during logic

optimization the overall cost of a concurrently checked circuit can be minimized This report presents a new technique called structure constrained logic optimization SCLO that optimizes a circuit under the constraint that faults in the resulting circuit can produce only a prescribed set of errors Using SCLO circuits can be optimized for various concurrent error detection schemes allowing the overall cost for each scheme to be compared A technique for quickly estimating the size of a circuit under different structural constraints is described This technique enables rapid exploration of the design space for concurrently checked circuits A new method for the automated synthesis of self checking circuit implementations for arbitrary combinational circuits is also presented It consists of an algorithm that determines the best parity check code for encoding the output of a given circuit and then uses SCLO to produce the functional circuit which is augmented with a checker to form a self checking circuit This synthesis method provides fully automated design explores a larger design space than other methods and uses simple checkers It has been implemented by making modifications to SIS an updated version of MIS Brayton 87a and results for several MCNC combinational benchmark circuits are given In most cases a substantial reduction in overhead compared to a duplicate and compare implementation is achieved **A Comprehensive Fault Model for Concurrent Error Detection in MOS Circuits** Daniel Lee Halperin,1984 Concurrent Error Detection with Latency in Sequential Circuits Lawrence Paul Holmquist,1989 **Error Detection and Location of Combinational Circuits** Yun-chung Cho,1970 **Adaptive Clocking and Dynamic Error Detection in Integrated Circuits** Suparna Das,2008 New Methods of Concurrent Checking Michael Gössel,Vitaly Ocheretny,Egor Sogomonyan,Daniel Marienfeld,2008-04-26 Computers are everywhere around us We for example as air passengers car drivers laptop users with Internet connection cell phone owners hospital patients inhabitants in the vicinity of a nuclear power station students in a digital library or customers in a supermarket are dependent on their correct operation Computers are incredibly fast inexpensive and equipped with almost unimag able large storage capacity Up to 100 million transistors per chip are quite common today a single transistor for each citizen of a large capital city in the world can be 2 easily accommodated on an ordinary chip The size of such a chip is less than 1 cm This is a fantastic achievement for an unbelievably low price However the very small and rapidly decreasing dimensions of the transistors and their connections over the years are also the reason for growing problems with reliability that will dramatically increase for the nano technologies in the near future Can we always trust computers Are computers always reliable Are chips suf ciently tested with respect to all possible permanent faults if we buy them at a low price or have errors due to undetected permanent faults to be discovered by c current checking Besides permanent faults many temporary or transient faults are also to be expected **A Phase Error Detection Circuit for a Carrier Synchronizer** Damon A. Rieth,Frank F. Cardin,New Mexico State University. Department of Electrical and Computer Engineering,1992 Configurable Array Logic Circuits for Computing Network Error Detection Codes Gordon Brebner,1991 **Official Gazette of the United States Patent and Trademark Office** ,1996 Official Gazette of the

United States Patent Office United States. Patent Office,1970   *Application of Residue Code in Automatic Error Detection and Correction in Logic Circuits* Fadi Y. Bu-Saba,1990   **Variation Tolerant Hierarchical Voltage Monitoring Circuit for Soft Error Detection** Ashay Narsale,2008   *Design of the Detector II: a CMOS Gate Array for the Study of Concurrent Error Detection Techniques* Stanford University. Computer Systems Laboratory,H. A. Goosen,M. L. Cortes,E. J. McCluskey,1987 For some applications of computer systems errors have to be detected concurrently with normal operation This is typically done by concurrent error detection CED circuits Since about 90% of errors in computer systems are caused by temporary failures CED schemes have to effectively detect errors caused by temporary failures Most CED schemes are designed with the assumption that errors are caused by events that can be modelled as single stuck faults There is a growing body of evidence which suggests that the single stuck fault model does not model temporary failures very well This report describes the Detector II a circuit which was designed to study concurrent error detection schemes experimentally The purpose of the study is to find out how well the different schemes perform in the presence of real temporary failures and to gain more knowledge of temporary failures in the process This will also lead to better models for temporary failures The circuit was implemented as a CMOS gate array fabricated by Fairchild Gate Array Milpitas California The circuit consists of approximately 2400 equivalent gates and is packaged in a 121 pin ceramic pin grid array package

Decoding **Error Detection Circuits**: Revealing the Captivating Potential of Verbal Expression

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